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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,765	09/10/2003	Yukiya Hirabayashi	116801	4078

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EXAMINER	
SCHECHTER, ANDREW M	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,765	HIRABAYASHI, YUKIYA	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11 February 2005 have been fully considered but they are not persuasive.

The applicant argues that *Young* does not disclose, nor would *Young* have suggested, a peripheral driving circuit being disposed at least partially within the sealed region. This is not persuasive. *Young* explicitly states that the peripheral driving circuits may be disposed within the sealed region [col. 9, lines 14-18].

The applicant argues that *Sawatsubashi* discloses and teaches [see Fig. 11] using a light shielding film [124] to cover the driver circuitry [113], so this should be taken as a teaching away from the amended limitation of claim 1 that "the common electrode and the light shielding film are in a non-overlapping arrangement with at least one of the peripheral driving circuit and wiring lines". This is not persuasive. The light shielding film [124] covers the driver circuitry [113] in only one embodiment in *Sawatsubashi* [not the embodiment relied on in the previous rejection]; since *Sawatsubashi* discloses other embodiments in which the driver circuitry is not overlapped by a light shield means, the reference should not be taken to "teach away" from having the driver circuitry not overlapped.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 2 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 2 recites the following limitations: the common electrode covers the entire surface of the counter substrate, and the peripheral driving circuit is disposed partially within the sealed region. Therefore, the peripheral driving circuit is overlapped by both the counter substrate and the common electrode. This does not contradict the additional limitation that counter substrate is in a non-overlapping arrangement with peripheral driving circuit or the wiring, since it can be non-overlapping with the wiring; however, it does not correspond to any figure in the specification, such an arrangement is never discussed, and it contradicts the repeated assertion that the advantage of the invention is to reduce or eliminate parasitic capacitance between the peripheral driving circuit and the common electrode. Therefore, the claim contains subject matter [namely, the counter electrode overlapping the peripheral driving circuit but not the wiring to the driving circuit] which was not described in the specification in such a way

as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 has been amended to recite "forming a common electrode and a light shielding film over an entire surface of a counter substrate; arranging [them] in a non-overlapping arrangement...". The intended scope of this limitation is unclear to the examiner. The light shielding film cannot be over the entire surface of the counter substrate in the finished product, or the device would be inoperable. Also, if the counter electrode is over the entire substrate and has the non-overlapping relationship, but the peripheral driving circuit is partially within the sealed region, the examiner does not see where support for such an embodiment is found in the specification. Presumably this is not the intent of the claim language. Does "arranging" mean that the common electrode and light shielding film are first formed on the entire surface, and then are patterned (removing parts thereof) so that they do not cover the entire surface, and are then in the non-overlapping arrangement? For examining purposes, this is assumed to be the case.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 5, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi et al.,* U.S. Patent No. 5,148,301 in view of *Shirahashi et al.,* U.S. Patent No. 5,285,301.

Sawatsubashi discloses [see Figs. 3-5] an electro-optical device comprising an active matrix substrate [101] having on the same plane a plurality of scanning lines [G1-Gm], a plurality of signal lines [D1-Dn] provided to intersect the scanning lines, a plurality of pixel electrodes [103] provided at the intersection portions of the scanning and signal lines, and a peripheral driving circuit [112, 113] to matrix drive the pixel electrodes; a counter substrate [102] having a common electrode [105] facing the pixel electrodes; a seal [108] that forms a sealed region between the substrate, with the peripheral driving circuit being disposed at least partially within the sealed region [see Figs. 3 and 4]; a liquid crystal layer [109] disposed in the sealed region between the active matrix substrate and the counter substrate; wherein the common electrode is in a non-overlapping arrangement with at least one of the peripheral driving circuit and wiring lines [114] for supplying signals to the peripheral driving circuit in plan view.

Sawatsubashi does not explicitly disclose a light shielding film on the counter substrate which is in a non-overlapping arrangement with at least one of the peripheral

driving circuit and wiring lines. *Shirahashi* discloses [see Fig. 15, for instance] a light shielding film [BM] on the counter substrate which is in a non-overlapping arrangement with at least one of the peripheral driving circuit and wiring lines [the black matrix covers only the dummy pixel regions and the non-display areas of the pixels]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a black matrix in the device of *Sawatsubashi*, motivated by the teaching of *Shirahashi* that it protects the semiconductor layers and clarifies the contour of each pixel to improve the contrast [col. 9, lines 9-45]. Claim 1 is therefore unpatentable.

Sawatsubashi's peripheral driving circuit comprises a data line driving circuit [112], and the wiring lines comprise clock signal lines and image signal lines [col. 5, lines 33-38], so claim 5 is also unpatentable. It is an electronic apparatus, so claim 7 is also unpatentable.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi et al.,* U.S. Patent No. 5,148,301 in view of *Shirahashi et al.,* U.S. Patent No. 5,285,301, as applied to claim 1 above, and further in view of *Yamamoto et al.,* U.S. Patent No. 5,506,705.

Sawatsubashi does not disclose single crystal silicon TFTs or driving signals to the peripheral driving circuit at a frequency equal to or more than 10 MHz. For an analogous LCD, *Yamamoto* discloses using single crystal silicon TFTs and a driving signal of 10 MHz [col. 12, lines 1-25]. It would have been obvious to one of ordinary skill in the art at the time of the invention to use single crystal silicon TFTs and a 10 MHz driving frequency in the device of *Sawatsubashi*, motivated by *Yamamoto's*

teaching that this allows high speed driving and thus improves the display quality. Claims 3 and 4 are therefore unpatentable.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Sawatsubashi et al.,* U.S. Patent No. 5,148,301 in view of *Shirahashi et al.,* U.S. Patent No. 5,285,301, as applied to claim 1 above, and further in view of *Segawa,* U.S. Patent No. 5,506,707, *Yamamoto et al.,* U.S. Patent No. 5,657,100, and *Kubota et al.,* U.S. Patent No. 6,355,314.

As discussed above, *Sawatsubashi* in view of *Shirahashi* discloses a method of manufacturing an electro-optical device, comprising forming a plurality of pixel electrodes [103] and a peripheral driving circuit [112, 113] to matrix drive the plurality of pixel electrodes on one surface of an active matrix substrate [101]; forming a common electrode [105] and light shielding film on one surface of a counter substrate [102] in a non-overlapping arrangement with at least one of the peripheral driving circuit and the wiring lines [114] for supplying signals to the peripheral driving circuit in plan view; bonding the active matrix substrate to the counter substrate with a predetermined gap using a sealing material [108] to form a sealed region, the peripheral driving circuit being disposed partially within the sealed region, and the common electrode facing the pixel electrodes; and forming a liquid crystal layer by injecting liquid crystal into the sealed region formed by the active matrix substrate, the counter substrate, and the sealing material [col. 4, lines 40-42].

Sawatsubashi in view of *Shirahashi* does not explicitly disclose forming the common electrode and light shielding film over the entire surface of the counter

substrate and then arranging [patterning – see discussion under 35 U.S.C. 112, 2nd paragraph, above] it as recited. *Sawatsubashi* in view of *Shirahashi* forms the same structure, but is silent on the method used to pattern these layers. There are two ways it could be done: 1) the recited technique, covering the entire counter substrate with the common electrode, and then removing the recited portion, or 2) using a deposition mask so that the material for the common electrode is only deposited in the desired regions, so nothing has to be removed (and similarly for the light shielding layer).

Segawa discloses making a counter electrode using the first technique, first sputtering ITO then etching it [col. 5, lines 10-29]. *Yamamoto* discloses making a counter electrode using the first technique, first sputtering and then etching [col. 4, lines 16-21]. *Kubota* discloses making a counter electrode using the first technique, first vacuum depositing the material then etching it [col. 37, lines 11-15]. It would have been obvious to one of ordinary skill in the art at the time of the invention to do it this way, motivated by the conventional nature of this technique (as evidenced by these references) which results in benefits to manufacturing time and cost from using existing production methods. Similarly, it would have been obvious to one of ordinary skill in the art at the time of the invention to use this technique to form and pattern the light shielding film, for the same reasons. Claim 6 is therefore unpatentable.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AS

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29 April 2005

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